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**SERIAL CONNECTED LOW-LOSS SYNCHRONOUSLY SWITCHABLE
VOLTAGE CHOPPER**

5 The present invention relates to a buck converter that, from a DC power supply voltage, allows another DC voltage of lower value to be obtained.

 New electronic components are being powered with lower and lower voltages (currently 2.5 V and 1.8 V,
10 and soon probably 1.2 V and 0.8 V) and the power requirements, at very low voltages, are increasing and becoming more important with respect to the conventional voltages +/-15 V and +5 V.

 The currents drawn are becoming increasingly
15 large since the power consumed by users is still the same or is increasing (capability for larger number of functions).

 Voltages below 3.3 V are not distributed and are installed directly on the user boards. The power supply
20 is being displaced as close as possible to the users.

 This tendency obliges power supply manufacturers to produce converters generating ever greater ratios between input voltage and output voltage.

 The structures used are generally pulse-mode
25 converters that are not isolated in order to maintain high efficiencies and converters with low dimensions. It is difficult for these converters, with a structure of the step-down type, to achieve a transformation ratio greater than 10 with efficiencies greater than
30 90%.

 In order to satisfy the demands of the market for higher levels of integration, these new converters must be deliverable within smaller and smaller surface areas and hence with increasingly higher efficiencies so as
35 not to increase the size of the power dissipators.

 The buck converter is one of the various converter structures.

Figure 1a shows a functional circuit diagram of a buck converter.

The circuit in Figure 1a is supplied by an input DC voltage V_{in} and delivers an output voltage V_{out} onto a load R_{out} in parallel with a capacitor C_{out} . A switch 10 allows either the positive potential of the input voltage V_{in} or the negative potential to be applied, for respective times T_{on} and T_{off} , to a terminal of an output inductor L_{out} that is connected by its other terminal to one of the load resistance terminals R_{out} . Figure 1b shows the closed time T_{on} and the open time T_{off} of the switch 10. The other terminal of the load resistance R_{out} is connected to the negative potential of the input voltage V_{in} . It will be assumed in the following that the negative potential of V_{in} is 0 volts.

The diagrams in Figures 1c, 1d and 1e show the operational principle of the buck converter.

It is assumed that the switch 10 is switched with a frequency of period T , with $T = T_{on} + T_{off}$ (see Figure 1c). The period T can be a constant or variable value.

The voltage V_I across the terminals of the inductor L_{out} is:

$V_I = V_{in} - V_{out}$, during the time T_{on} and
 $V_I = -V_{out}$, during the time T_{off} .

The mean voltage V_m of the output voltage V_{out} across the terminals of the resistance R_{out} will therefore be in the range between V_{in} and 0 volts depending on the duty cycle T_{off}/T and will be given by $V_m = (T_{on}/T) \cdot V_{in}$.

The mean value V_m of the voltage V_{out} is constant. The current I_{lout} in the inductor L_{out} takes the form of ramps during the times T_{on} and T_{off} . A diode D ensures the continuity of the current in the inductor during the switching operations.

In the diagram in Figure 1c the case of $T_{on} = T/2$ and hence $V_{out} = V_{in}/2$ is shown.

The diagrams in Figures 1d and 1e respectively show two values of mean voltage V_{m1} and V_{m2} across the terminals of the load resistance R_{out} for two values of the time T_{on} :

- 5 - in the diagram in Figure 1d: $T_{on}/T = 0.9$
and,
- in the diagram in Figure 1e: $T_{on}/T = 0.1$.

In other words, when T_{on}/T is small, the energy supplied by the power source, during the short time
10 T_{on} , is small, producing a low mean voltage across the terminals of the load. On the other hand, when T_{on} is close to the period T , the load is virtually continuously connected to the power source, the mean output voltage is close to the DC input voltage.

15 In another type of operation of the buck converter, the time T_{on} is kept constant and the switching frequency, in other words the switching period T , is changed so that the ratio T_{on}/T is made to vary.

20 In practice, the switches are formed by two semiconductors in series, for example two MOS switches controlled by complementary signals at the frequency $1/T$.

The buck converters of the prior art nevertheless
25 have limitations. Indeed, a duty cycle T_{on}/T of 0.1 is the minimum that can currently be obtained with an acceptable performance in terms of efficiency and reliability. However, when it is desired to obtain an output voltage lower than one tenth of the input
30 voltage, the conduction time T_{on} of the semiconductor supplying the energy to the load becomes very short and the switches become very difficult to control. In addition, if the output voltage decreases, for a given power delivered to the load, the currents in the
35 semiconductors become large, at the limits of their capabilities, with a loss of efficiency of the converter.

Another means for obtaining a ratio between the input voltage and the output voltage that is much

higher than 10 consists in forming a voltage step-down device comprising two cascaded converters. In this device, the output voltage of a first converter is applied to the input of a second converter. Thus, much
5 higher ratios between the input voltage and the output voltage of the device can be obtained than those obtained by a single converter. Nevertheless, such a step-down device comprising two cascaded converters exhibits a globally lower efficiency than that of a
10 single converter and a higher cost of production.

In order to overcome the problems of the buck converters of the prior art, the invention proposes a buck converter comprising:

- a pair of input terminals A and B for
15 connecting an input DC voltage V_{in} across these two terminals, the potential of the terminal A being higher than the potential of the terminal B;

- a pair P_0 of switches SB, SH in series and connected to the input terminal B by the switch SB,
20 each switch SB, SH comprising a control input so that, simultaneously, one is set in a conducting state by the application of a first control signal at its control input, and the other in an isolating state by the application of a second control signal, complementary
25 to the first control signal, at its control input;

- a pair of output terminals C and D for supplying a load R_{out} with an output voltage V_{out} , the output terminal D being connected to the input terminal B and the output terminal C to the connection point
30 between the two switches SB and SH in series via a filter inductor L_{out} , characterized in that it comprises:

- K other additional pairs $P_1, P_2, \dots, P_i, \dots, P_{K-1}, P_K$ of switches in series between the input
35 terminal A and the switch SH of the pair P_0 , with $i = 1, 2, \dots, K-1, K$, the two switches of the same additional pair P_i being connected in series via an energy recovery inductor L_{r_i} ;

- K input groups, $Gin_1, Gin_2, \dots, Gin_i, \dots, Gin_{K-1}, Gin_K$, of N_i capacitors C in series, each of the same value, with $i = 1, 2, \dots, K-1, K$ and $N_i = (K+1) - i$, the electrode of the capacitors of one of the two
5 ends of each input group $Gin_1, Gin_2, \dots, Gin_i, \dots, Gin_{K-1}, Gin_K$ being connected to the input terminal A, at least the electrode of the capacitors of each of the other ends of the input groups $Gin_1, Gin_2, \dots, Gin_i, \dots, Gin_{K-1}, Gin_K$ being connected to the
10 connection point between two pairs of consecutive switches $P_{(i-1)}$ and P_i , respectively;

- K output groups, $Gout_1, Gout_2, \dots, Gout_i, \dots, Gout_{K-1}, Gout_K$, of M_i capacitors C in series, each of the same value, with $i = 1, 2, K$ and $M_i = i$, the
15 electrode of the capacitors of one of the two ends of each output group $Gout_1, Gout_2, \dots, Gout_i, \dots, Gout_{K-1}, Gout_K$ being connected to the common point between the two switches of the pair P_0 , at least the electrode of the capacitors of each of the other ends
20 of the output groups $Gout_1, Gout_2, \dots, Gout_i, \dots, Gout_K$ being connected to the common point between each switch SH_i and the recovery inductor Lr_i of the corresponding pair P_i of the same rank i , respectively,

25 in that the switches of these other K additional pairs are simultaneously controlled by the first and second complementary control signals forming, when the switch SB of the pair P_0 connected to the terminal B is set in the conducting state for a time T_{off} , a first
30 network of capacitors connected between the terminal A and the terminal B, comprising the groups of input capacitors in series with the groups of output capacitors such that a group of input capacitors Gin_i is in series, via its respective energy recovery
35 inductor Lr_i , with its respective group of output capacitors $Gout_i$,

and in that, when the switch SB of the pair P_0 connected to the input terminal B is set in the isolating state, SH being set in the conducting state,

for a time T_{on} , these other K pairs of switches form a second network of capacitors, connected between the terminal A and the output filter inductor L_{out} , comprising the input group G_{in_1} in parallel with the
5 output group G_{out_K} , in parallel with input capacitor groups in series with output capacitor groups such that an input capacitor group G_{in_i} is in series with an output capacitor group G_{out_i} .

The voltage V_{out} at the output of the converter
10 depends on the duty cycle T_{on}/T , and since the network capacitors C have the same value, the voltage V_{out} is given by the equation:

$$V_{out} = V_{in} \cdot (T_{on}/T) \cdot 1/(K+1)$$
 with a chopping
frequency of the input voltage V_{in} of period $T = T_{on} +$
15 T_{off} .

The invention will be better understood with the aid of exemplary embodiments according to the invention, with reference to the indexed drawings, in which:

20 - Figure 1a, already described above, shows a functional circuit diagram of a voltage step-down buck converter;

- Figures 1b, 1c, 1d and 1e show control state diagrams of the converter in Figure 1a;

25 - Figure 2 shows the general structure of the converter according to the invention comprising K additional pairs of switches;

- Figure 3 shows a structure of a buck converter comprising two pairs of switches without the recovery
30 inductors L_{r_i} ;

- Figure 4 shows the converter from Figure 3 in a more realistic configuration;

- Figure 5 shows the losses in watts in the case of the converter in Figure 3 supplied by an ideal
35 voltage source and by a real source;

- Figure 6 shows the curves of the losses in watts for various output voltages V_{out} of the converter in Figure 4;

- Figure 7 shows the power loss variations in Figure 5 expressed as a percentage of the power delivered by the converter;

5 - Figure 8 shows the power loss variations in Figure 6 expressed as a percentage of the power delivered by the converter;

10 - Figure 9a shows a converter according to the invention in a structure comprising two pairs of switches and in the more realistic configuration of Figure 4;

 - Figure 10 shows an equivalent circuit diagram of the converter in Figure 9a according to the invention during the period T_{off} ;

15 - Figure 11 shows the control signals of the switches of the converter in Figure 9a during the times T_{off} and T_{on} ;

 - Figure 12 shows, during the time T_{off} , the variation of the current I_{lr_1} in the energy recovery inductor L_{r_1} ;

20 - Figure 13 represents energy space showing the energy in the recovery inductor L_{r_1} versus that in the capacitances C_e , C_s of the converter;

25 - Figure 14 shows the variation of the value of the voltage V_{in} across the terminals of the converter according to the invention;

 - Figures 15 and 16 show two practical structures of the buck converter according to the invention;

 - Figure 17 shows a variant of the buck converter in Figure 9a according to the invention.

30 Figure 2 shows the general structure of the converter according to the invention comprising K additional pairs of switches. The converter in Figure 2 also comprises the current return diode D across the terminals of the switch SB whose anode is connected on the side of the terminals B and D , and an output filter capacitor C_{out} in parallel with the load R_{out} between the output terminals C and D .
35

 In the general structure of the converter according to the invention in Figure 2, the voltages V_c

across the terminals of the capacitors of the input groups or of the output groups have the same DC value, thus the capacitors situated at the same potential level can be connected together.

5 In order to explain the improvement in the efficiency of the buck converter according to the invention brought about by the recovery inductors L_{r_i} , connected between the two switches of each of the additional pairs, in a first step of this explanation,
10 Figure 3 shows a buck converter structure comprising two pairs of switches without the recovery inductors L_{r_i} , the switches of each pair being, in this case, directly connected in series, the power supply voltage V_{in} being assumed to come from an ideal generator E_p
15 whose voltage is independent of the current drawn.

 The converter in Figure 3 comprises two pairs P_0 and P_1 , each of the pairs having two switches connected in series, the switches S_B , S_H for the pair P_0 and the switches S_{B_1} , S_{H_1} for the additional pair
20 P_1 . Each switch of a pair comprises a control input so as to simultaneously set one of them in a conducting state by applying a first control signal C_1 at its control input, and the other in an isolating state by applying a second control signal C_2 , complementary to
25 the first control signal, at its control input.

 In order to explain the operation of the converter in Figure 3, the capacitance of the input group G_{in} will be denoted by C_e and the capacitance of the output group G_{out} by C_s .

30 At the start of the conduction phase of the switches S_H and S_{H_1} of each of the two pairs, the voltage V_{ce} across the terminals of the input capacitance C_e and the voltage V_{cs} across the terminals of the output capacitance C_s are equal to $V_{in}/2$, C_e and
35 C_s having the same value equal to C_1 .
 At the end of the conduction phase, V_{ce} and V_{cs} are still equal but their values become:

$$V_{ce} = V_{cs} = \frac{V_{in}}{2} + \frac{1}{C_1} \cdot \frac{I_{out}}{2} \cdot t_{on}$$

with I_{out} : current in the load resistance R_{out} of the converter

T_{on} : conduction time of SH and SH_1

5 During the next conduction phase of the switches SB and SB_1 of the two pairs (T_{off}), the sum of the voltages across the terminals of the capacitances C_e and C_s is brought back to the same value with:

10
$$V_{ce} = V_{cs} = \frac{V_{in}}{2}$$

There is therefore a loss of energy caused by the resistive re-balancing of the capacitances C_e and C_s via the switches SB and SB_1.

15 The re-balancing losses increase with the current drawn I_{out} and with the duty cycle.

These losses are given by the equation (1):

$$P(w) = \frac{I_{out}^2 \cdot V_{out}^2}{F \cdot C_1 \cdot V_{in}^2}$$

20 with:

$V_{in} = 32$ volts

$V_{out} = 5$ volts

$I_{out} = 10$ amps

$C_1 = 10$ microfarads

25 $F = 350$ kHz

The losses amount to 1.163 watts for an output power of 50 watts, which is about 2.3% of the output power.

30 Figure 4 shows the converter from Figure 3 in a more realistic configuration. Indeed, the converter power supply comprises the voltage generator E_p in series with an input inductor L_{in} , representative of the inductance of the power supply connections, and an input filter capacitor C_{in} in parallel across the two
35 input terminals A and B of the converter.

In this configuration in Figure 4, the same rise in the voltages V_{ce} and V_{cs} on the respective capacitances C_e and C_s is observed during the conduction phase of the switches SH and SH_1 , with in addition a decrease in the voltage across the terminals of the input capacitor C_{in} of:

$$\Delta V_{cin} = -\frac{I_{out}}{C_{in}} \cdot t_{on}$$

During the closed phase of SB and SB_1 , there is also a resistive (and hence dissipative) re-balancing of C_{in} , C_e and C_s .

The re-balancing losses in the case of the more realistic converter in Figure 4 are given by the equation (2):

$$P(w) = \frac{F}{2} \left[C_{in} \left(V_{in} - \frac{2 \cdot I_{out} \cdot V_{out}}{F \cdot C_{in} \cdot V_{in}} \right)^2 + \frac{C_l}{2} \left(V_{in} - \frac{2 \cdot I_{out} \cdot V_{out}}{F \cdot C_l \cdot V_{in}} \right)^2 - \left(C_{in} + \frac{C_l}{2} \right) \left(V_{in} - \frac{2 \cdot I_{out} \cdot V_{out}}{F \cdot C_{in} \cdot V_{in}} + \frac{C_l + C_{in}}{2 \cdot C_{in} + C_l} \cdot \frac{2 \cdot I_{out} \cdot V_{out}}{F \cdot C_{in} \cdot V_{in}} \right)^2 \right]$$

20

with:

$V_{in} = 32$ volts
 $V_{out} = 5$ volts
 $I_{out} = 10$ amps
25 $C_{in} = 6$ microfarads
 $C_l = 6$ microfarads
 $F = 350$ kHz

The losses amount to 3.1 watts for an output power of 50 watts, which is 6.2% of the output power, hence a loss that is three times higher than in the case of the circuit with ideal power supply in Figure 3.

It will be noted that the limit of this equation (2) when C_{in} tends to infinity is the equation of an ideal input voltage V_{in} . In practice, it is the size

35

and the cost of the input filter capacitor C_{in} that are the limiting factors. In a practical system, there will essentially be a loss three times as high as in the theoretical case shown in Figure 3.

5 This result with $K=1$ may be generalized to converters comprising more than one additional pair.

Figure 5 shows the losses $P(w)$ in watts as a function of the output current I_{out} in the load R_{out} for a voltage V_{out} of 5 volts.

10 The curve $C_p(w)$ in Figure 5 shows the losses in watts in the case of the converter in Figure 3 supplied by an ideal voltage source. The curve $C_r(w)$ in the same Figure 5 shows the losses in watts in the case of the more realistic converter in Figure 4.

15 Figure 7 shows the variations in the power losses in Figure 5 expressed as a percentage of the power delivered by the converter. Curves $C_p(\%)$ and $C_r(\%)$.

In the case of Figures 5 and 7, the losses $P(w)$ are calculated for the following parameter values:

20 $V_{in} = 32$ volts
 $V_{out} = 5$ volts
 $I_{out} = 10$ amps
 $C_{in} = 6$ microfarads
 $C_l = 6$ microfarads
25 $F = 350$ kHz, F being the chopping frequency of the converter.

Figure 6 shows the curves of the losses $P(w)$ in watts for various output voltages V_{out} of the more realistic converter in Figure 4, the other parameters
30 being identical to those of the embodiment in Figure 3.

Figure 8 shows the variations in power losses in Figure 6 expressed as a percentage of the power delivered by the converter.

Figure 9a shows a converter according to the
35 invention in a structure comprising two pairs of switches and in the more realistic configuration of Figure 4 for the power supply. The power supply, delivering the supply voltage V_{in} of the converter, comprises the voltage generator E_p in series with the

input inductor L_{in} and the filter capacitor C_{in} in parallel between the two input terminals A and B of the converter.

5 The converter in Figure 9a comprises the pair P_0 having the two switches SB and SH connected in series and the additional pair P_1 having the two switches SB_1 and SH_1 connected in series via an energy recovery inductor Lr_1 .

10 In the following, the operation of the buck converter in Figure 9a according to the invention will be explained.

Figure 10 shows an equivalent circuit diagram of the converter in Figure 9a according to the invention during the period T_{off} , corresponding to the conduction
15 period of the switches of the two pairs SB and SB_1 . During this time T_{off} , the switches SB and SB_1 are closed, the switches SH and SH_1 are open, the input capacitor C_{in} is in parallel with the two capacitances C_e and C_s which are in series with the recovery
20 inductor Lr_1 .

The recovery inductor Lr_1 is calculated so as to obtain a resonance of the oscillating circuit in Figure 10 such that:

25
$$T_{off} = \pi \sqrt{Lr_1 \cdot C_{eq}}$$

with

$$C_{eq} = \frac{1}{\frac{1}{C_{in}} + \frac{1}{C_e} + \frac{1}{C_s}}$$

It is considered that T_{off} is constant and equal
30 to around the half-period of the resonance frequency of the equivalent circuit in Figure 10.

Figure 11 shows the control signals of the switches of the converter in Figure 9a during the times T_{off} and T_{on} .

35 Figure 12 shows, over the time T_{off} , the variation of the current I_{lr_1} in the energy recovery inductor Lr_1 together with the sum of the voltages

($V_{ce} + V_{cs}$) across the terminals of the respective capacitances C_e and C_s .

At time t_1 , when going from T_{on} to T_{off} , the current in the inductor is zero, the voltage ($V_{ce} + V_{cs}$) across the terminals of the capacitances C_e and C_s is higher than the mean value V_{inm} of V_{in} and decreases through the mean value of V_{in} , the current in the inductor increases while storing magnetic energy, goes through a maximum value when ($V_{ce} + V_{cs}$) goes through the mean value of V_{in} , then the current decreases down to a value of zero, corresponding to the end of T_{off} , returning the energy to the capacitances C_e and C_s . The current in the inductor becomes zero, the sum of the voltages ($V_{ce} + V_{cs}$) increases, during the time T_{on} , to above the mean value of V_{in} , then the cycle commences again at the start of T_{off} .

Figure 13 represents energy space showing the energy in the recovery inductor Lr_1 versus that in the capacitances C_e , C_s of the converter. The abscissa represents the capacitance energy W_c , the ordinate the energy in the inductor W_{lr_1} , the energy variation between the inductor and the capacitances taking place in the time T_{off} . During this phase T_{off} , the variation of the energy in the capacitances and in the inductor produces a small variation in the mean value of the voltage V_{in} . The energy is transferred from the capacitances toward the recovery inductor then returned to the capacitances.

The tuning of the converter circuit at the frequency of operation with the recovery inductor Lr_1 considerably reduces the resistive losses in the buck converter circuit according to the invention. These losses then become practically zero.

Figure 14 shows the variation in the value of the voltage V_{in} across the terminals of the converter according to the invention.

During the time T_{off} , the voltage V_{in} varies according to ($V_{cs} + V_{ce}$),

from $+\Delta v$ to $-\Delta v$, then during T_{on} the voltage varies from $-\Delta v$ to Δv as a function of the output current I_{out} ; this variation is given by the equation (3):

5

$$\frac{I_{out}}{2} \cdot \frac{dt}{CI}$$

In addition, in order to make the converter according to the invention more reliable, the buck converter shown in Figure 9a comprises, in parallel with the pair P_1 , a diode Sc_1 in series with an impedance Z_1 , the anode of the diode Sc_1 being connected to the connection point between the pair P_1 and the lower pair P_0 , the common point between the cathode of the diode Sc_1 and the impedance Z_1 being connected to the connection point between the switch SB_1 and the recovery inductor Lr_1 .

Indeed, in practice, the T_{off} does not perfectly represent the resonance half-period of the equivalent circuit in Figure 10, and the impedance Z_1 allows the residual current to be dissipated and the switches, which are generally MOS transistors, to be protected. The diode Sc_1 is a 'flywheel' diode.

This improvement of the converter in Figure 9a is applicable in the general case, where each additional pair P_i of the converter according to the invention comprises, in parallel, a diode Sc_i in series with an impedance Z_i , the anode of the diode Sc_i being connected to the connection point between the pair P_i and the lower pair P_{i-1} , the common point between the cathode of the diode Sc_i and the impedance Z_i being connected to the common point between the switch SB_i and the recovery inductor Lr_i .

The impedance Z_i comprises, in a first version shown in Figure 9b, a diode Dd in series with a resistor r , the anode of the diode Dd being connected, in the converter circuit, to the cathode of the diode Sc_i and, in a second version shown in Figure 9c, the

impedance Z_i comprises the diode D_d in series with a zener diode D_z , the two cathodes of the diode D_d and the zener diode D_z being connected together, the anode of the diode D_d being connected, in the converter
5 circuit, to the cathode of the diode Sc_i .

The 'flywheel' diodes Sc_1, \dots, Sc_i , the diode D ensuring the current continuity in the output inductor L_{out} and the diodes D_d of the impedances Z_i can, for certain embodiments of the converter, be silicon diodes
10 and, for other embodiments, Schottky diodes.

The explanation of the operation of the buck converter comprising the recovery inductor Lr_1 with two pairs ($K = 1$) remains valid for any number of K additional pairs. Indeed, since the number of
15 elementary capacitors C in the groups connected in series by the switches are the same, the currents in the various pairs P_i and in the corresponding recovery inductor Lr_i are the same.

This general structure shown in Figure 2 allows
20 various other practical structures to be formed simply and the value of the capacitors in each input or output branch to be determined directly.

Indeed, as has been stated previously, in the general structure in Figure 2 comprising capacitors C
25 of the same value, the voltages V_c across the terminals of each of the capacitors are the same for the input groups and the same for the output groups, and consequently, the capacitors of the same potential level can, either in part or as a whole, be connected
30 in parallel.

The capacitors of the same potential level Nin_1 are, for example, all those of the input groups $Gin_1, Gin_2, \dots, Gin_i, \dots, Gin_{K-1}, Gin_K$ having one electrode connected to the input terminal A, of a potential level
35 Nin_2 , all those connected by one electrode to the free electrodes of the capacitors of the level Nin_1 and by the other electrode to those of the next level Nin_3 , and so on up to the level Nin_K .

Similarly, for the capacitors of the output groups, there will be the level Nout_1 for all those of the output groups Gout_1, Gout_2,...Gout_i,...Gout_K-1, Gout_K connected to the common point between the two
5 switches of the pair P_0, of a potential level Nout_2 all those connected by one electrode to the free electrodes of the capacitors of the level Nout_1 and by the other electrode to those of the next level Nout_3, and so on up to the level Nout_K.

10 The dashed lines on the circuit diagram in Figure 2 represent the possible connections between the capacitors C of the same value.

In a first practical structure, shown in Figure 15, not comprising interconnections between the capacitors of the same potential level, each of the
15 input groups Gin_i or output groups Gout_i respectively comprises a single capacitance Cea_1, Cea_2;... Cea_i... Cea_K for the input group Gin_i and Csa_1, Csa_2;...Csa_i... Csa_K for the output groups Gout_i.
20 The value of each of these input capacitances Cea_i can be simply deduced from the general structure by the calculation of the resultant capacitance of Ni = (K+1)-i capacitors C in series, with i = 1, 2,...K, i being the order of the input group in question:

$$\begin{aligned}
 & \text{Cea}_1 = C/K & i = 1 \\
 & \text{Cea}_2 = C/(K-1) & i = 2 \\
 & \dots \\
 & \text{Cea}_i = C/((K+1)-i) & i \\
 & \dots \\
 & \text{Cea}_K = C & i = K
 \end{aligned}$$

The value of each of these output capacitances Csa_i can be simply deduced from the general structure
35 by the calculation of the resultant capacitance of Mi = i capacitors C in series, i being the order of the output group in question:

$$\text{Csa}_1 = C \quad i = 1$$

$$\begin{array}{ll}
 \text{Csa}_2 = C/2 & i = 2 \\
 \dots & \\
 \text{Csa}_i = C/i & i \\
 \dots & \\
 5 \quad \text{Csa}_K = C/K & i = K
 \end{array}$$

In a second practical structure shown in Figure 16 comprising the interconnections between the capacitors of the same potential level N_v (capacitors in parallel), the structure comprises a single input group G_{in} and a single output group G_{out} . The input capacitance of each of the potential levels N_{in_i} , i being the order of the potential level in question at the input, in parallel with its respective pair P_i will be simply deduced by calculating the capacitance C_{eb_i} equivalent to the capacitors in parallel of the level N_{in_i} in question, which is:

$$\begin{array}{ll}
 C_{eb}_1 = C.K & i = 1 \\
 20 \quad C_{eb}_2 = C.(K-1) & i = 2 \\
 \dots & \\
 C_{eb}_i = C.((K+1)-i) & i \\
 \dots & \\
 25 \quad C_{eb}_K = C & i = K
 \end{array}$$

The output capacitance of each of the potential levels N_{out_i} , in parallel between two consecutive pairs pair P_i , P_{i-1} , will be simply deduced by calculating the capacitance C_{sb_i} equivalent to the capacitors in parallel of the level N_{out_i} in question, i being the order of the output potential level in question, which is:

$$\begin{array}{ll}
 C_{sb}_1 = C.K & i = 1 \\
 35 \quad C_{sb}_2 = C.(K-1) & i = 2 \\
 \dots & \\
 C_{sb}_i = C.((K+1)-i) & i \\
 \dots & \\
 C_{sb}_K = C & i = K
 \end{array}$$

In other embodiments, the two types of practical
embodiments may of course be combined by putting
capacitors in parallel for certain groups and in series
5 for others.

Figure 17 shows a variant of the buck converter
in Figure 9a according to the invention. In this
variant, the recovery inductor L_{r1} is replaced by a
transformer Tr_1 whose primary is connected in place of
10 the recovery inductor between the two switches of the
first additional pair P_1 , the secondary being
connected, at one end, to the terminals B and D of the
converter and, at the other end, to the input terminal
A via a zener diode Zb_1 whose cathode is connected to
15 said input terminal A.

In this variant, the transfer of energy stored in
the inductance of the transformer Tr_1 occurs toward
the power supply source (capacitor C_{in}) and not toward
the link capacitors C as in the case of the embodiment
20 in Figure 9a.

In a general case, the embodiment in Figure 17 is
applicable to a converter comprising more than one
additional pair; the converter then comprises K
recovery transformers, the primary of a transformer of
25 order Tr_i being connected between the two switches of
the additional pair P_i , the secondary being connected,
at one end, to the terminals B and D of the converter
and, at the other end, to the input terminal A via a
zener diode Zb_i whose cathode is connected to said
30 input terminal A.

In another variant, the transfer of energy stored
in the recovery inductor occurs toward the output load
 R_{out} ; the converter according to the invention
comprises K recovery transformers, the primary of a
35 transformer of order Tr_i being connected between the
two switches of the additional pair P_i , the secondary
being connected, at one end, to the terminals B and D
of the converter and, at the other end, to the output
resistance R_{out} via a zener diode Zb_i whose cathode is

connected to said output resistance, the transfer of energy stored in the recovery inductor occurring toward the output load R_{out} .

5 The buck converter according to the invention
allows efficiencies that are significantly higher than
the efficiencies of the converters of the prior art to
be obtained with voltage ratios V_{out}/V_{in} less than
1/10. In practice, efficiencies better by around 6%
with respect to the prior art buck converter are
10 obtained with structures that are adaptable to the
various industrial cases and are simple to implement.